Ultra-high I/O Density Glass/Silicon Interposers for High Bandwidth Smart Mobile Applications

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Abstract

Smart mobile applications are driving the demand for higher logic-to-memory bandwidth (BW) in 10-30 GB/s range with lower power consumption and larger memory capacity. This paper presents a radically-different, scalable and lower cost approach than the 3D ICs with TSV stack approach being pursued widely, to achieve high bandwidth. This approach is referred to as interposer approach using ultra-thin glass or silicon with ultra-high I/O density interposers, which does not require TSVs in the logic IC in the 3D stack. This paper presents a comparative study, based on electrical modeling of the logic-to-memory signal path, in various current and emerging package configurations for use in smart mobile devices. Frequency and time domain analysis for each of these scenarios is performed using both chip and package-level models with varying interconnection dimensions. Simulated eye diagrams for the complete data paths in the thin glass interposer approach demonstrated more than 3 Gbps/pin data rate, similar to 3D ICs.

I. Introduction

A combination of graphics, games and memory-intensive applications is expected to accelerate the demand for memory-to-logic bandwidth in both mobile and high performance applications [1]. This trend imposes significant barriers to packaging schemes, due to realistic low power and low cost budgets. Packaging schemes such as package-on-package (PoP) and wire-bonded SiP (System-in-Package) are limited in bandwidth due to their long interconnection lengths and low I/O density. Vertical stacking using newer PoP schemes [2], [3] and horizontal mounting using silicon interposers [4], [5], [6], [7] have been proposed to tackle the bandwidth challenge. Further, double-sided stacking using advanced organic interposers has also been demonstrated for reducing latency and improving performance [8].

However, these are limited either due to the IC-to-interposer CTE mismatch, via-pitch scalability, electrical loss or cost. Recently, wide I/O bus using interconnected logic and memory in a single 3D IC stack with through-silicon-vias (TSVs), has begun to emerge as the primary technology of choice for high bandwidth in next generation smart phones. Such logic and memory 3D IC designs typically have four DRAM dies and a single logic die, bonded either face-to-face or face-to-back using TSVs, as shown in Figure 1. While this presents an exciting and unparalleled opportunity to achieve ultra-high bandwidth, this 3D IC approach with TSV imposes grand challenges in low cost TSV formation in the wafer factory, power delivery, testability, reliability, and cooling in the 3D stack [9], [10], [11].

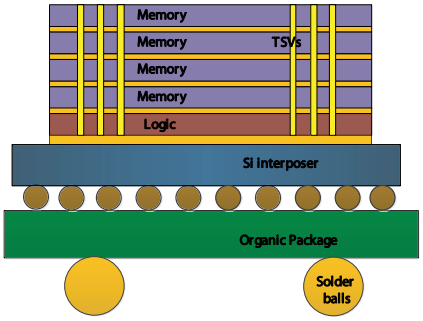

Fig. 1. Emerging approach based on 3D IC with TSVs

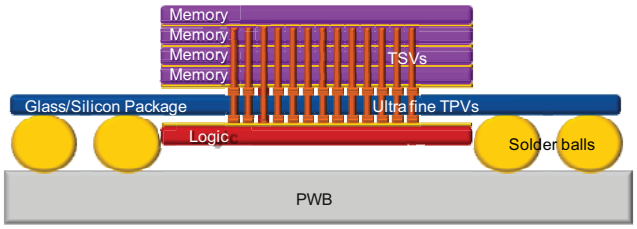

Fig. 2. High memory-to-logic bandwidth using double-sided glass/Si interposers

This paper proposes an alternative approach that is scalable, testable and lower cost to achieve high bandwidth using an interposer with ultra-short interconnection length and ultra-high interconnection density between logic IC on one side and memory stack ICs on the other side of the interposer, by so called double-side interconnection, as shown in Figure 2. This interposer can be made of ultra-thin silicon or glass or even organic substrate. A comparative study based on comprehensive electrical modeling of the logic-to-memory signal path in four different package approaches is presented as shown in Figure 3: (1) wire-bonded System-In-Package (SiP), (2) Package-on-Package (PoP), (3) 3D IC with TSVs, and (4) Interposer-based TPVs. In 3D IC with TSV configurations, two variations were considered based on bonding: (1) face-to-face bonding between logic and memory (3DIC-F2F), and (2) face-to-back bonding between logic and memory (3DIC-F2B).

Similarly, in the case of interposer-based through-package-via (TPV) configurations, where TPVs are the vertical vias that are found in the interposers for signal and power delivery (= same role as TSVs in 3D ICs), four variations were considered

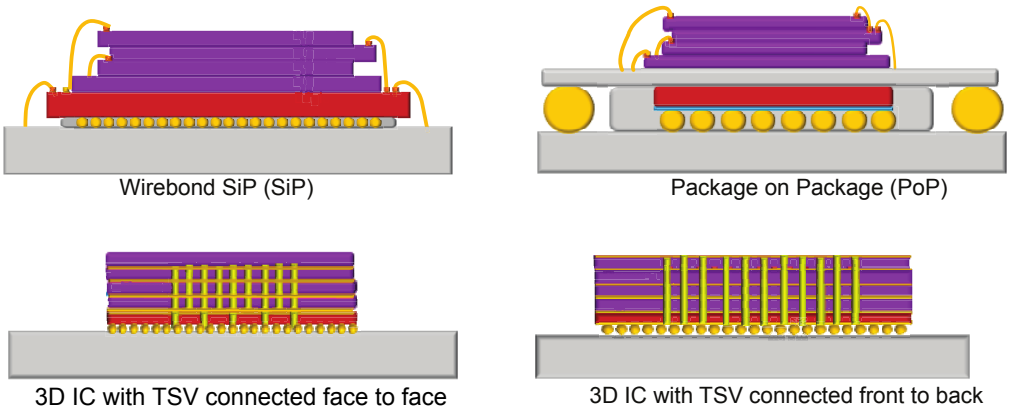

Fig. 3. Various 3D interconnect approaches between logic and memory

TABLE I. Specifications of various system integration technologies used in our study

Different integration technologies	Attributes
Wirebonded-SiP (SiP)	Single hop is assumed to connect each die. Bond wires are modeled based on AmKor specifications at 1 mil diameter and 65μm pitch [12]
Package on Package (PoP)	Memory package is on the top of the logic package. JEDEC specifications were considered [13]. Accordingly, top package has a 4L stackup, and the bottom has a 2L stackup.
3D IC with F2F connection between memory and logic (3DIC-F2F)	F2F connection height is assumed to be negligible, and this is represented by 40μm on chip wire between the dies.
3D IC with F2B connections between all dies (3DIC-F2B)	Each TSV is assumed to be 50μm in height and 5μm in diameter.
Double side stacking using proposed 30μm thick glass interposer (ultra-thin glass)	5-10μm polymer is assumed on either side of the glass. The through-package-via (TPV) is 50μm high and 10μm in diameter.
Double side stacking using 180μm thick glass interposer (thin glass)	20μm polymer is assumed on either side of glass. TPVs are 220μm high and 30μm in diameter.
Double side stacking using conventional single crystalline Si interposers (Si interposer)	Thickness of sidewall liner is 0.1μm. TSV is 30μm in diameter and 200μm in thickness.
Double side stacking using panel based polycrystalline silicon with a sidewall containing 5μm polymer lining (Panel Si)	Surface polymer lining of 20μm on either side of silicon is assumed. TPV is 30μm in diameter and 200μm in height

based on thickness and material for the interposer (1) Conventional Si interposer with 0.1μm liner thickness (Si interposer), (2) Polycrystalline Si with 5μm polymer liner (Panel Si), (3) Thin glass interposer with 180μm glass thickness (Thin glass), and (4) Ultra-thin glass interposer with 30μm glass thickness (ultra-thin glass). Delay analysis based on the above models is carried out. Frequency and eye diagram simulations are also carried out to demonstrate the effectiveness of the interconnects found in these system integration options.

II. Benefits of Ultra-high I/O, Ultra-short Interconnection in Double-side Interposers

Table II presents a comparison between the typical dimensions of 3D IC with TSVs and the proposed interposer-based thin glass. There are several advantages for the proposed interposer approach as listed in Table III, some of which are presented in other works [14]:

- Low cost of making large number of through-package vias (TPVs) in ultra-thin glass compared to TSV by DRIE
- Fabrication of ultra-thin glass in large panel sizes, not requiring chemical-mechanical polishing
- Ultra low loss of glass, with better signal insulation and without insulation liner compared to TSV in Si for 3D ICs
- Ultra-high I/O density with 20-30 micron pitch TPVs, similar to TSV in Silicon
- Testability of interposer, interposer with logic, and interposer with logic and memory
- Scalability in both horizontal and vertical dimensions
- Improved thermal management of logic ICs

TABLE II. Typical interconnect dimensions in 3D IC vs ultra-thin glass interposer

Parameter	3D IC with TSVs	Ultra-thin glass interposer
Diameter	4-50μm	5-20μm
TSV/TPV pitch	10-80μm	10-40μm
Thickness	20-250μm	30-50μm
RDL wiring Lines/Space	.5-2μm	5-10μm

TABLE III. Comparison of system metrics between 3D IC and ultra-thin glass interposer

Metrics	3D IC with TSVs	Ultra-thin glass interposer
Bandwidth	high	high
Reliability	med	high
Latency	low	low
Watt/bit	low	low
Scalability	low	high
Flexibility	low	high
Cost	high	low

One major concern with the interposer approach, however, is the power delivery due to longer power delivery path to the logic die. Potential solutions to this problem include multiple metal layers of power and ground islands, which are integrated within the interposer. As a result, a lower-resistance path can be provided to the power delivery network (PDN) of the die. Table III provides a comparison between 3D IC with TSVs vs. Interposer-based approach with glass or silicon. Efficient power and thermal designs with thin glass interposers are being investigated and will be reported in the future.

III. Electrical Modeling and Analysis Methodologies

In order to facilitate meaningful comparison among the interconnects used in various system integration options shown in Table I, we design and analyze source-to-sink signal paths from these options based on two different scenarios: a worst case model and a best case model. The objective is to compare six different configurations that are used to integrate four memory dies and one logic die, as shown in Figures 2 and Figure 3. The logic die is placed at the bottom in all configurations. Figure 4 shows the structural models for each interconnect structure used in our study for time and frequency domain analysis.

Figure 6 shows the design flow used in this study. Nangate 45nm open cell library was used to create the input and output buffers [15]. Since buffers are generally placed close to the on-chip I/O pads, the on-chip interconnection was modeled as 20μm in length. On-chip interconnects were modeled using a simple distributed pi model based on 45 nm technology parasitics. Separate models for top and bottom package (for PoP), as shown in Figure 5, were created in SONNET. The TSVs and TPVs were modeled in CST Microwave Studio, a 3D full wave EM solver. The depletion region was modeled using the analysis presented in [16]. Finally, schematics for each scenario were designed using ADS and the delay was computed at 50% voltage. A PCI express standard was used to determine the criterion for signal transmission. All interconnects were matched to 50 ohms terminations and their frequency and time responses were studied.

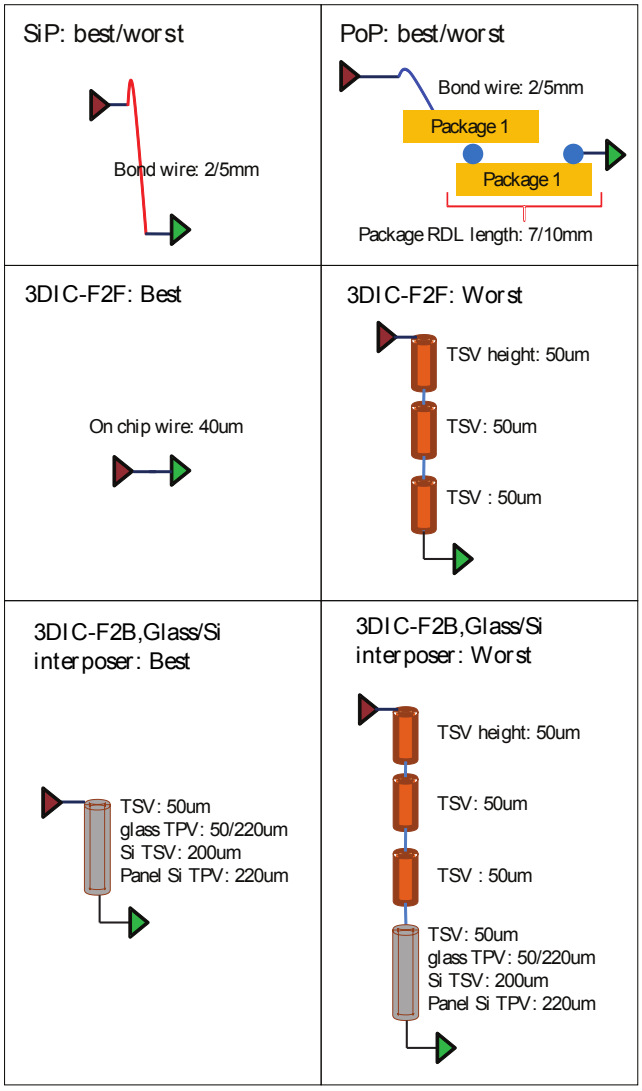

Fig. 4. Overview of the best and worst case interconnection structures

IV. Simulation and Measurement Results

A. Time Domain Analysis: Delay

Time domain analysis was performed for the models described in the previous section. For smart mobile applications, logic-to-memory channel frequency of 400 MHz is being proposed to operate a wide-I/O data bus. This aims to save power while achieving high bandwidth. This paper primarily uses this frequency to characterize the delay. Every signal path was simulated with different buffer sizes in order to determine

TABLE IV. Memory-logic interconnection path delay (in ps)

	1 GHz 64X, 1.1V		400 MHz 64X, 1.1V		400 MHz 64X, 1.0V		400 MHz 32X, 1.1V		400 MHz 32X, 1.0V	
	Best	Worst	Best	Worst	Best	Worst	Best	Worst	Best	Worst
Wirebond	113	147	114	147	127	160	145	171	162	212
PoP	252	321	251	314	273	357	396	525	459	578
3DIC-F2F	81	114	80	114	88	128	83	139	95	173
3DIC-F2B	98	126	99	125	111	141	102	156	121	196
Ultra-thin Glass	85	117	81	190	92	131	86	141	102	177
Panel Si	107	126	107	125	118	151	123	191	147	215
Thin Glass	158	200	184	200	179	215	206	258	215	276
Si Interposer	–	–	288	322	356	394	–	–	–	–

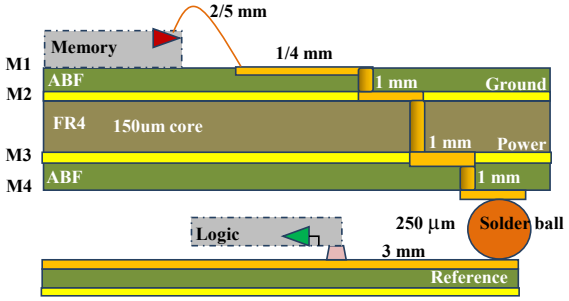

Fig. 5. Interconnection path in Package-on-Package logic-memory integration

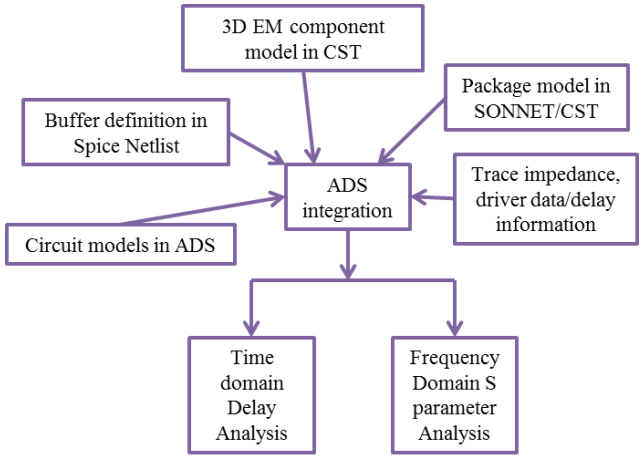

Fig. 6. Flowchart for the analysis methodology

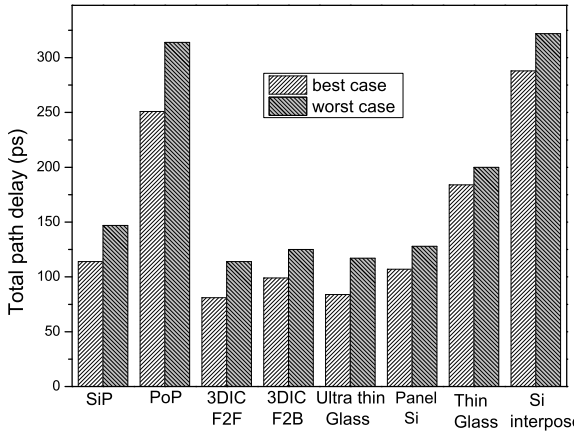

Fig. 7. Memory-logic interconnection delay with 64X buffer, 1.1 V

TABLE V. Impact on delay due to additional dies in the memory-logic interconnection path (in ps)

64X, 1.1V 400 Mhz	2 Die stack	# Additional Dies		
		1	2	3
3DIC-F2B	81	98	114	125
Si Interposer	288	302	315	322
Ultra-thin Glass	81	91	100	109
Panel Si	107	110	118	126

the load characteristics. The effect of the driving voltage (1 V and 1.1 V) and frequency (400 MHz and 1 GHz) on the path delay was also studied. Two buffer sizes: 32X and 64X were used for this analysis.

Table IV shows the results of this study. The variation in delay was negligible with the change in frequency. As shown in Figure 7, there was significant variation in the delay across various configurations. The worst case delay in PoP and Si interposers was more than 300 ps. In PoP, this was due to the latency of the long redistribution lines (RDL) present in the package. In silicon interposer, this was mainly due to the large capacitance associated with the 200μm high TSV (with 100 nm sidewall Silicon dioxide liner). Figure 8 shows the delay comparison when driven by a 32X buffer. The maximum output capacitance that can be driven by the 32X buffer is 819 fF. Hence the input driver does not have sufficient drive capacity in the case of silicon interposer, due to output load parasitics that are above this limit. The delay increases with decrease in the driving voltage for the buffers. Comparing the 3D IC with TSV approaches with the interposer approaches, it was seen that that 3DIC-F2F and thin glass interposers performed the best, having approximately 100 ps delay. Panel-based (for low cost) silicon interposers performed much better

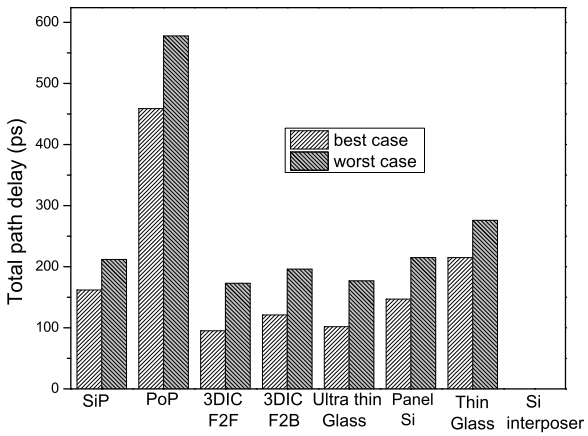

Fig. 8. Memory-logic interconnection delay with 32X buffer, 1 V

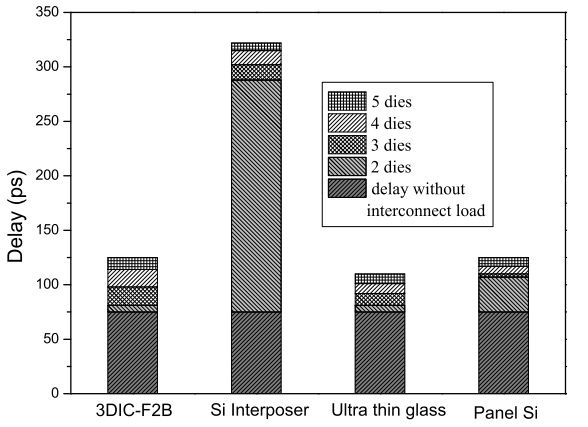

Fig. 9. Effect of IC loading on total path delay

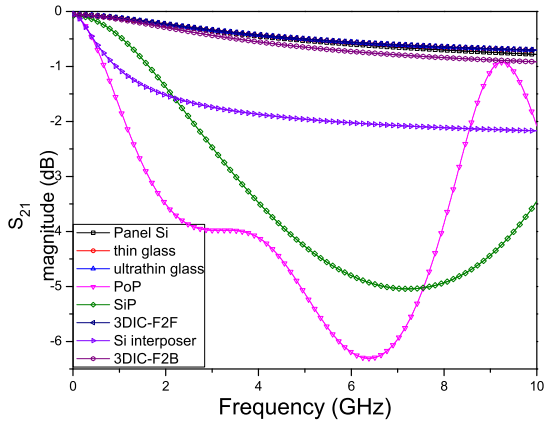

Fig. 10. Insertion loss for worst case interconnection path length

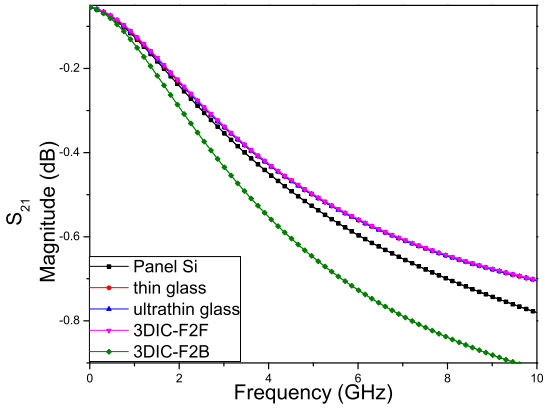

Fig. 11. Insertion loss for low-loss integration approaches (worst case)

than wafer-based silicon interposers (with thin sidewall silicon dioxide liner) due to reduced capacitance. Except the case of the silicon interposer, performance of other interconnects models (in 3D IC approaches and interposer approaches) were dominated by the buffer.

The change in delay with the addition of each individual die to the stack was also analyzed. The 64X buffer delay (without any interconnect load) was found to be 75 ps. The logic IC was connected to a single memory IC and the corresponding increase in delay was noted for the different 3D IC and interposer approaches. Subsequently memory ICs were added incrementally and the increase in delay was determined. Table V and Figure 9 summarizes this study result.

In the case of 3D ICs with TSVs and glass interposers, the total delay was dominated by the buffer delay when the system consisted of just one memory IC connected to a logic IC. As additional memory ICs (with TSVs) were added, the total delay increases depending on the path parasitics. In case of silicon interposer, the delay due to intrinsic interconnect capacitance dominated the overall delay. Addition of successive ICs with TSVs continued to increase the delay in a more gradual manner. It was observed that in the case of TSVs and TPVs, migration towards smaller dimensions reduced latency.

B. Frequency Domain Analysis: S-Parameter

S-parameter comparisons for silicon and glass interposer has been presented in [16]. In this work, the entire data path between the memory and logic IC was simulated for worst and best case interconnect lengths. From Figures 10, 11, 12, and 13, it is observed that 3DIC-F2F has the best response, which is followed closely by glass and panel-based silicon interposers. This is due to the low loss in high resistivity glass substrate, and due to the thick polymer TPV liner in panel- based silicon inteposers. The PoP and wirebond SIP packages suffer from variations in their responses due to long interconnect lengths and large inductance.

C. Signal Transmission Line Simulations

Logic-to-memory data rates of 3 Gbps/pin or more has been studied for different applications [17]. Time domain simulations were performed for thin glass interposers with TPVs. A

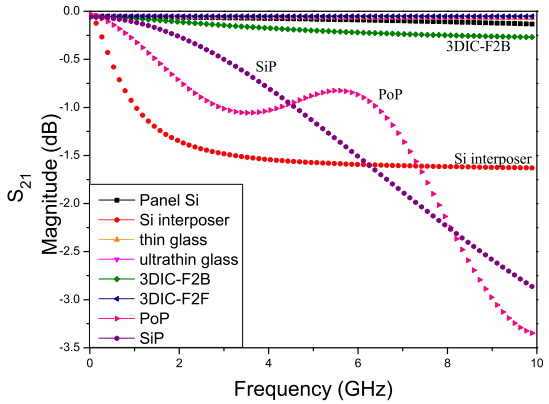

Fig. 12. Insertion loss for best case interconnection path length

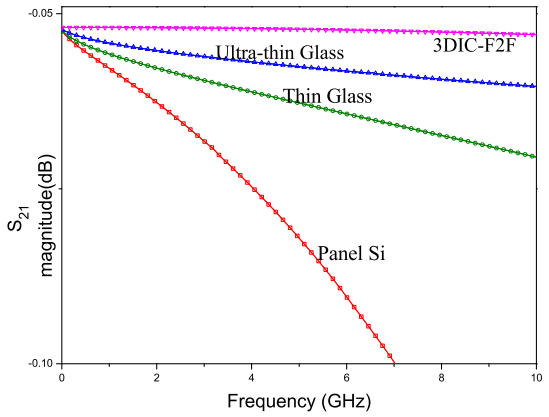

Fig. 13. Insertion loss for low-loss integration approaches (best case)

single ended configuration using a CPW configuration (10μm line width) was used for this simulation. For the high speed PCI-express connection, eye height greater than 505 mV and a width of atleast 250 ps is needed. The signal path was simulated at 3 GHz and the eye width and height were noted. These specifications were met in both the worst (318 ps, 931 mV) and the best case (264 ps, 964 mV) with thin glass interposers. To determine the performance of TPV with long redistribution lines on the interposer, a thin glass interposer with 6 mm RDL (3 mm on each side) was simulated. Figure 14 shows the eye response of this path at 3 GHz. The set specifications were again met in this case which showed that the interposer was capable of supporting high speed buses running between adjacent stacks.

D. Glass Interposer Test Vehicle Design and Measurement

Small vias in glass and silicon interposers have been demonstrated in [18]. Test structures were designed and fabricated to characterize the signal loss through the interconnections (RDL lines and TPVs) in glass interposer. Figure 15 shows the cross-section view of a CPW line to TPV transition structure.

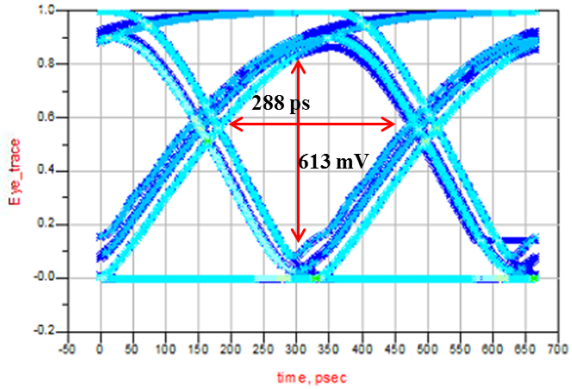

Fig. 14. Simulated eye diagram for thin glass with 6 mm RDL at 3 GHz signal with 64X, 1 V

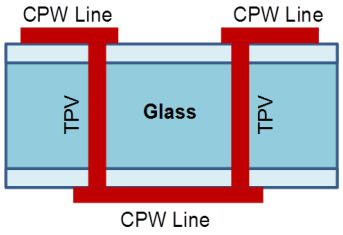

Fig. 15. Cross section schematic of a CPW line - TPV transition structure[14]

The glass thickness was 180μm and trace line lengths on each layer of the test vehicle structure was 0.5 mm. 2-port VNA measurements were performed with microprobes, after SOLT calibrations. The comparison between the measured and simulation data is shown in Figure 16. It was observed that the simulation results match closely with the measurement results. The interconnection path had low insertion loss (less than 0.15 dB) till 9 GHz. The complete details on the test vehicle and fabrication process are presented in [14].

V. Summary and Conclusion

An alternative, scalable, testable and lower-cost approach to 3D ICs with TSV to achieve high bandwidth between logic and memory ICs was proposed, studied and reported. This alternative is based on the use of ultra-thin glass or silicon interposer with ultra-high I/O density interconnection, with logic on one side and memory on the other side. Delay modeling of these interposer interconnections showed very low latencies, indicating its capability to provide high-quality signal paths. The simulation results were validated by close correlation with measured data from a test vehicle with small pitch TPVs in glass interposer. Eye diagrams generated by the time domain simulations demonstrate high speed data transmission capabilities over 3 Gbps/pin, similar to 3D logic and memory ICs with TSV. This enables the new interposer-based approach to achieve bandwidth similar in magnitude to 3D ICs but with the potential to be a lower cost, more scalable,

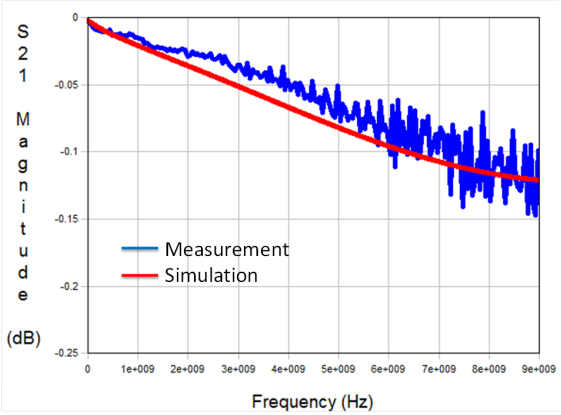

Fig. 16. Insertion loss plot of a CPW line - TPV transition structure[14]

and more testable and easier to manage the thermal challenges than the 3D IC approach being pursued widely.

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